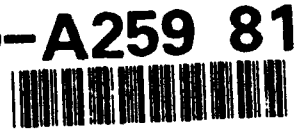

AT&T Bell Laboratories

subject: **AT&T OETC quarterly technical report for October-December 1992**

date: **January 8, 1993**

from: **J. L. Zilko**
Org. AT&T
Breinigsville,Pa. 2A-201
215-391-2582

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J. L. Zilko

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1. Overview of activities during October-December 1992

The activities of October-December 1992 have primarily revolved around detailed design of the AT&T transmitter and receiver and associated pieceparts and in performing initial experiments to determine the feasibility of the design approach.

1.1 Task A.1: VCSEL fabrication

On the basis of the several month long epitaxy and process optimization experiment and transmission experiments by IBM on AT&T-supplied SEL's (described below), a first iteration SEL design has been decided upon. This design is nominally single mode (time averaged side mode suppression of < -40 dB) with both low lasing threshold current (I_{th} ~ 3-6 mA at room temperature) and threshold voltage (V_{th} < 2.5 V). We have also demonstrated a relatively weak temperature dependence of I_{th} for any given laser with a typical 2 mA difference in I_{th} between 0 and 60° C). The dependence of peak power output on temperature is somewhat larger (P_{pk} decreases by ~ 2.5X between 0 and 60° C). It should also be noted that although the lasing wavelength varies from wafer to wafer and across wafers due to the extreme sensitivity of this parameter to small differences in layer thickness, the light-current-voltage characteristics do not appear to be dependent on the lasing wavelength over a rather large 30 nm lasing wavelength window, suggesting that the design and fabrication process are sufficiently robust for a reproducible, high yield device.

In collaboration with IBM, AT&T SEL's of both single mode (SM) and multimode (MM) designs were used in transmission experiments in order to better define the proper SEL design for the OETC application. The single mode SEL's and the multimode SEL's at sufficiently low bias exhibit a single fundamental mode with a well defined radially symmetric Gaussian beam and a $1/e^2$ divergence angle of 18°. At higher

biases, the multimode SEL exhibits higher order modes which are often donut shaped but can be multilobed. Even in the multimode case, however, the divergence of the higher order modes are contained within a 20° full angle. We will discuss coupling of single and multimode layers further in the discussion on the progress on Task A.2.

The transmission experiments indicated that the use of multimode SEL's results in more coupled power headroom because multimode SEL's emit more power than single mode SEL's. This is useful if the bit error rate is limited by received power. However, the multimode SEL's are slower than the single mode SEL's and and the laser turnon delay is much more sensitive to bias in the multimode SEL's than the single mode devices. As a result, very tight threshold uniformity requirements are put on the multimode elements across the array in order minimize skew due to variations in turnon delay.

Although faster and less sensitive to skew, the use of single mode SEL's was demonstrated to result in a bit error rate floor (in the 10^{-7} to 10^{-6} range) when the SEL was subjected to mode selective loss in the transmission experiment, thus indicating a potential model noise problem. The modal noise occurred despite a < -40 dB side mode suppression ratio in the time averaged spectrum and was speculated to result from instantaneous mode shifts under modulation. The primary way of eliminating this as a source of system noise is anticipated to be through a reduction in mode selective losses in the optical packaging.

From the above transmission experiments, it was decided to use the single mode device. For this device design, a series of Version I laser specifications have been agreed to by AT&T, IBM, and GE. These specifications follow:

Property	Interchip	Intrachip
Operating temperature (° C)	0-60	± 5
Wavelength (nm)	835-855	± 2
Threshold current (mA)	3-6	± 20%
Threshold voltage (V)	< 4	± 20%
10 mA voltage (V)	< 5	-

10 mA power (MM) (mW)	> 1	-
10 mA power (SM) (mW)	> 0.5	-
$\Delta\lambda/\Delta T$ (A/° C)	0.6	-
Bias current (mA)	6 ± 1	-
Modulation current (mA)	5 ± 1	-

The Version 1 OETC-specific SEL mask design has been completed and masks have been delivered. The mask set allows for a 1 X 32 element array of SEL's for data transmission, a number of alignment marks for use in subsequent packaging, 100 X 300 μm bonding pads, alignment marks and traces for two monitor SEL's and photodiodes on the outer portions of the chip, and a backside metalization grid consisting of metal dots for solder attachment self-alignment to a Si submount. The chip size is 9 mm X 2.5 mm and is constrained by the necessity of allowing space for the two monitor photodiodes and by the aspect ratio requirements of robust die separation.

The mask set will contain three primary patterns: one a standard OETC chip, a second standard OETC chip with full surface backside metalization (to be discussed more fully in the Task A.2 section below), and the third for alignment marks and test structures to be used for wafer failure mode analysis. The number of primaries of each kind are listed below:

Pattern	50 mm wafer	75 mm wafer
Primary 1 (OETC)	49	124
Primary 2 (OETC with full surface metal)	6	11
Primary 3 (Test structures)	11	18

The Version I mask set will be used for producing standard OETC chips for both initial deliveries and in order to explore distributions and reproducibility of laser results. In addition, the mask set will be used as a vehicle for making SEL process improvements in order to improve devices performance and yields.

From the above discussion, milestone 3, Task A.1, Tested Laser Chip Available has been fulfilled.

1.2 Task A.2: Transmitter packaging

The optical subassembly (OSA) fiber coupling concept that was discussed in the last quarterly report was experimentally verified by measuring coupling efficiency of single and multimode SEL's into 45° angle polished multimode fiber. For these experiments, the polished fiber had no mirror attached to it so that rather large (~ 30%) transmission loss occurred through the fiber end that would not occur in our proposed OETC coupling design. However, by measuring relative coupling efficiency, these experiments did allow measurement of the tolerance of coupling efficiency to alignment variations and the differences in coupling efficiency between single mode and multimode devices.

The results of the coupling efficiency experiments indicate good coupling efficiency (measured to be ~ 60%, would have been ~ 90% with a mirror) for both single and multimode SEL's over a reasonably wide positional tolerance range. The single mode devices gave somewhat better (~ 5%) coupling than the multimode SEL's. This is due to the relatively poorer coupling of the donut shaped higher order mode which contains a significant amount of multimode emitted power compared to the Gaussian fundamental mode. Both single and multimode devices suffered a degradation of coupling efficiency of < 5% for misalignments of ± 10 μm in both lateral dimensions (along and across the fiber length) while the single mode SEL suffered a 5% degradation as the distance between the SEL and fiber increased from 0 μm to 100 μm. The multimode SEL showed little (~ 5% between 0 and 100 μm) degradation of coupling with increasing distance between SEL and fiber when operated at low bias where it was single mode, while suffering a considerably larger 20% degradation between 0 and 100 μm SEL-fiber separation when operated at higher bias where it was multimode.

The lateral misalignments (± 10 μm) and SEL-fiber separations (0 - 100 μm) for which little coupling degradation was measured are within the alignment and separation tolerances that we expect to achieve in assembling our OSA. This increases our confidence in the technical feasibility of our design approach.

Two monitor Si photodiodes have been provided in the package design in order to set SEL power levels and to account for variations in SEL parameters with temperature and with aging. The photodiode chips are 1.1 mm X 1.1 mm and have a 500 μm diameter active area. They have been designed to be bonded directly on top of the SEL chip over two special monitor SEL elements. This design has the advantage of allowing

non-critical monitor diode chip placement while maintaining reproducible and good coupling of light between the monitor SEL's and the photodiodes which should, in turn, result in reproducible photocurrent response from the photodiodes.

Although no saturation of the photodiode with small spot sizes was detected for a spot size as small as 10 μm, we intend to use a several hundred micron thick spacer between the the SEL's and the photodiodes in order to enlarge the light spot to well above 10 μm. One concern about the photodiode placement is the likely optical feedback to the SEL from reflections from the photodiode surface. If this proves to be a problem, we will work to provide a solution that would reduce reflections into the SEL.

The package design calls for the self-aligned solder attachment of the SEL chip to a Si submount. A fiber coupler part is then accurately aligned to the SEL position through the use of photolithographically defined matching grooves that are etched into the Si submount and the Si fiber coupler pieces. Thus, the accuracy of the SEL-fiber alignment will be largely determined by the accuracy of the solder self-alignment process. Although we believe, from separate experiments, that ± 5 μm alignment accuracy is possible with with our proposed solder attach process, we want to have three alignment degrees of freedom (two lateral and one angular) in assembling the initial transmitter OSA rather than the single lateral degree of freedom that the solder and etched groove process allows in order to compensate for worse than expected alignment accuracy or piecepart design errors. For this reason, we will not use etched grooves for submount-fiber coupler alignment in the initial transmitter model, but will align using three degrees of freedom onto a non-grooved Si submount. Although not compatible with low cost manufacturing, this approach will allow considerable experience in other aspects of transmitter assembly and should reduce the risk in delivering the first mechanical transmitter model. After obtaining data on placement accuracy for our solder attachment process and other aspects of our transmitter design, we would then introduce the use of alignment grooves, considered a relatively low risk technological addition, to the second iteration transmitter assembly in order to demonstrate this technology.

The self-alignment process uses matching metal and solder dots in a grid pattern on the backside of the SEL and the frontside of the Si submount, respectively. Because our present solder deposition and patterning technology allows the use of only thin solder, we are limited to a dot size that is small and a

pitch that is relatively large in order achieve the solder thickness that is necessary for a robust solder attach process. This results in a limited attachment contact area between the SEL and the Si submount. Calculations that we have done indicate that this could result in a significant increase in SEL thermal resistance. The Primary 2 chip that was mentioned in the discussion of Task A.1 is the standard OETC chip with full surface backside metal, which will be used to investigate the thermal resistance penalty due to the present solder bump pattern.

In parallel, we plan to develop a process for the second iteration transmitter that will allow the direct deposition of solder that is of the correct thickness for robust bonding. Deposition of thick solder will allow a much smaller solder bump pitch which will greatly increase SEL chip contact to the Si submount and decrease the thermal resistance of the SEL chip.

Work continues to define the hybrid package into which the transmitter OSA and the driver chips will be placed. We plan to mount the OSA, consisting of the SEL chip, fiber connector piece, and Si optical bench parts, and the receiver chip, not part of the OSA, into the high speed ceramic package which contains 50 Ω termination resistors and decoupling capacitors as well as electrical traces to the pins.

Electrical connections will be made by wire bonding from the SEL to metal traces on the ceramic. Because of the desire to interleave ground and signal bonds to minimize electrical crosstalk and because the ground and signal bonds come from two levels of the OSA (top of the SEL chip for signal, bottom of the SEL/top of the Si submount for the ground), we have decided to provide an electrical fanout of the 32 signal lines (at 140 μm pitch) and 12 interleaved ground lines through wire bonds to traces on ceramic at 140 μm pitch. These traces go to the driver IC from GE in a manner to be determined (because the IC I/O has not been determined). The traces then go through the termination resistors and decoupling capacitors to the pins. As will be discussed in the update on Task A.3, a thermal analysis has been done on a version of the ceramic package.

Milestone 3, Task A.2, Package Design, Version 1 Complete, has been fulfilled.

Milestone 4, Task A.2, Packaged Laser Array, Version 1, scheduled for December 1992, has not been fulfilled, but was originally inappropriately scheduled for this time. Since Milestone 3, Task A.2 was only

completed (on time) in November 1992, it is unreasonable to expect the Packaged Laser Array to be completed before many of the pieceparts have been designed and fabricated. A more appropriate time for this milestone is May 1993 which is what we will use for the purposes of this contract.

1.3 Task A.3: Receiver packaging

Our receiver package design is similar in many respects to that planned for the transmitter, described above in the A.2 section. There are, however, several exceptions. Our original intent was to perform a self-aligned solder attach, similar to that which we are planning for the SEL. This requires backside metalization and patterning. However, the foundry that IBM is using for fabricating the receiver chips does not have any backside processing capability. In addition, they use Al metallurgy, which is incompatible with performing a solder attach with AT&T's Au metallurgy that is used for the Si submount.

We have considered the possibility of performing backside processing on IBM receiver wafers in order to provide the appropriate pattern for self-aligned solder attach. However, due to concerns about the risk of damaging the receivers thermally and mechanically by performing backside patterning (ideally, a process like this should occur before, not after receiver fabrication) and the development costs that AT&T would incur to develop fixtures for the receiver wafer size and process development, it was decided to epoxy rather than solder the receiver chip to the Si submount. Although this decision means that we will be using a high cost (although sufficiently capable) manufacturing process for receiver attach and will not be able to demonstrate self-alignment with the receiver chip, we will still be able to demonstrate self-aligned chip solder attachment technology using the SEL chip.

The use of Al and Au metallurgies for the receiver chip and package, respectively, leads to an additional concern in wire bonding with either Al or Au wire. After some investigation, we have concluded that although void formation in the metal couple might result in long term reliability concerns, mixing Al and Au should not result in any short term deleterious effects for this program.

The use of a differential output from the receiver chip means that we need to bond on pads with a 70 μm pitch (0.5X the optical pitch). Two bonding configurations were considered: one in which the bond pads are in two rows and staggered which effectively doubles the pitch to 140 μm, and a single row of pads

at 70 μm pitch. Although the ability to accurately and rapidly bond to staggered bond pads is enhanced due to the large pad size, concern was raised about the possibility of shorting bond wires together. The use of a single row of pads at 70 μm pitch coupled with state-of-the-art bonding equipment reduces that probability of wire bond shorting but requires care in setting up the placement of the bond onto the considerably smaller pads. This is an especially large burden for a large number of bonds. Because the number of bonds that need to be made to provide differential output is limited to 64, it was decided to use the single row of bond pads at 70 μm pitch for the differential output. Power and ground bonds, made on other edges of the chip, will be to standard size pads.

Partially in response to a request from IBM, a rather detailed thermal analysis was performed on the receiver package that is proposed for this program. This package is similar to the transmitter package, but is larger in order to accommodate the higher thermal dissipation of the receiver. The package is a 124 I/O module with a ceramic footprint of 38.1 mm X 38.1 mm and a package foot print of 45.2 mm X 45.2 mm. The receiver OSA is bonded directly to the heat spreader and it was assumed that little heat was conducted by the pins to the printed wiring board. The analysis indicates a thermal impedance of ~ 2.5 C/W from the receiver-submount interface to the submount-heat spreader interface. The thermal resistance from the submount-heat spreader interface to the ambient adds an additional 24 to 13 C/W for air cooling velocities from 6.7 tp 91 l/min. This information has been transmitted back to IBM.

Milestone 2, Task A.3, Package Design Complete, was completed this past quarter.

1.4 Task A.4: Fiber connector

Pieceparts for fabricating 32 fiber jumper cables have been ordered, including Si pieces for MAC connectors, fiber, and cabling of the fiber. A number of Si pieces have been delivered and a small number have been sent to Honeywell to assist them in the design of their modulator package. 19,000 m of fiber was delivered to the cabling vendor for cabling into 32 fiber cable. Unfortunately, the cabling vendor had unanticipated manufacturing problems that have delayed delivery of cable and which destroyed a significant amount of cable (200 m of the planned 500 m). Cable delivery has been rescheduled for January 8, 1993 at which point we should receive 300 m. Although this is anticipated to be sufficient for this program, we would expect little leftover cable.

Milestone 2, Task A.4, Acquire Fiber, has been fulfilled.

Milestone 3, Task A.4, First Model, has not been fulfilled due to the above problems with cable manufacture and delivery. We anticipate fulfilling this milestone by the end of January and do not believe that missing this milestone will impact future deliveries or milestones.

1.5 Task A.5: Project Management

Considerable time and effort has been spent in monitoring progress on this program and coordinating the efforts both within AT&T and between AT&T, IBM, GE, and Honeywell. Four intercompany meetings have been held to discuss OETC technical issues: one at AT&T, Murray Hill, New Jersey, with Honeywell, one at AT&T, Murray Hill, New Jersey with IBM, one at AT&T, Breinigsville, Pennsylvania with IBM, and one at IBM, Yorktown Heights, New York, with IBM and GE. The meeting with Honeywell discussed ways in which AT&T could help Honeywell package their modulator so that it is compatible with the AT&T MAC connector in keeping with the spirit of the OETC proposal.

2. Anticipated activity for January-March 1993

2.1 Task A.1: VCSEL fabrication

It is anticipated that the first OETC-specific SEL wafer will be fabricated and will be in the process of device characterization.

2.2 Task A.2: Transmitter packaging

It is anticipated that Si optical bench pieceparts will be in fabrication, that the HIC design will be complete, and that the transmitter test set will be in fabrication.

2.3 Task A.3: Receiver package

It is anticipated that Si optical bench pieceparts will be in fabrication and that the HIC design will be complete.

2.4 Task A.4: Fiber connector

It is anticipated that the first connectorized 32 fiber cable and 8 additional jumper cables will be

available for this program.